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EXAMINER	
CUTLER, ALBERT H	
ART UNIT	**PAPER NUMBER**
2622	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/765,930	KASUGA, SHIGETAKA	
	Examiner	Art Unit	
	Albert H. Cutler	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8 and 10-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10,12,13 and 15* is/are allowed.

6)☒ Claim(s) *1 and 16* is/are rejected.

7)☒ Claim(s) *2-6,8,11 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is responsive to communication filed on August 8, 2007.

Response to Arguments

2. Applicant's arguments filed August 8, 2007 have been fully considered but they are not persuasive.

3. Applicant argues, "The present invention relates to a solid state imaging device using N-type MOS transistors alone included therein as transistors, as recited by Claim 1. On the other hand, the image sensor of Gowda et al. relates to a CMOS image sensor where both N-MOS and P-MOS transistors are utilized. For example, a peripheral part of the image sensor includes a signal processing circuit, a timing and control logic circuit and a column select/scan logic which comprise CMOS circuits (see FIG. 3; col. 1, line 17 - col. 2, line 9; and col. 2, lines 61-65). Therefore, Gowda et al. fail to disclose a solid state imaging device using N-type MOS transistors alone as transistors.

4. The Examiner respectfully disagrees. Claim 1 calls for, "A solid state imaging device using N-type MOS transistors alone". However, claim 1 also requires, "a scanner for selecting and reading said digital signal". Upon examination of the present application, the Examiner has been unable to find a scanner using N-type MOS transistors alone in the specification and drawings. Because the disclosure does not illustrate a scanner using N-type MOS transistors alone, the Examiner concludes that not all of the external circuitry associated with the pixel array must be comprised of N-type MOS transistors alone.

5. Thus, the Examiner interprets said "solid state imaging device using N-type MOS transistors alone" to be the pixel array(i.e. a solid state imaging device) of Gowda et al.(see figure 3), which pixel array comprises N-type MOS transistors alone(see figure 4, column 5, lines 12-13). Although the external circuitry associated with the solid state imaging device(i.e. pixel array) taught by Gowda et al. may comprise transistors other than N-type MOS transistors, this is a moot point as the external circuitry in the form of the scanner taught in the current application has not been clearly illustrated as containing N-type MOS transistors alone.

6. Therefore, the Examiner is maintaining the rejection.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

9. Claim 1 recites, "A solid state imaging device using N-type MOS transistors alone as transistors therein". However, claim 1 also requires, "a scanner for selecting and reading said digital signal". Upon examination of the present application, the Examiner has been unable to find a scanner using N-type MOS transistors alone in the

specification and drawings. Therefore, a person having ordinary skill in the art at the time of the invention would not have been enabled to make the claimed N-type MOS solid state imaging device containing a scanner.

Claim Rejections - 35 USC § 102

10. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

11. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Gowda et al.(U.S. Patent 6,115,066).

Consider claim 1, Gowda et al. teach:

A solid state imaging device(figures 3 and 4) using N-type MOS transistors alone as transistors included therein(Column 5, lines 12-13, figure 4), comprising:

a pixel unit(image sensor, 20, figure 3) composed of a plurality of pixels(30) arranged in a two-dimensional matrix(see figure 3), each of said pixels(30) including a photoelectric converting element(26, figure 4) for generating charge in response to light(26 is a photodiode, column 4, lines 23-25.) and an amplifying element(23, figure 4) for outputting, as an analog signal, a voltage signal corresponding to said charge generated by said photoelectric converting element(FET 23 provides a signal directly related to(i.e. an amplified signal) the charge on the photodiode, column 6, lines 19-22.);

a selection signal line(15, figure 3) provided correspondingly to each pixel row(see figure 3) of said pixel unit(20);

a comparison/storage unit(40 and 42, figure 3) provided correspondingly to each pixel column(see figure 3) of said pixel unit(20) for converting, into a digital signal, said analog signal output from said amplifying element(23) included in each pixel(30) belonging to a pixel row selected in said pixel unit(30, see figure 3) and for storing said digital signal(Each pixel row contains an ADC(40) for converting the analog signal into a digital signal, column 6, lines 22-26. This digital signal is then stored in a register(42), column 6, lines 24-26.);

a scanner(44, figure 3) for selecting and reading said digital signal stored in said comparison/storage unit in time series(column 6, line 28 through column 7, line 20); and

an amplifier(44, figure 3) for amplifying said read digital signal and outputting said amplified digital signal to the outside(The "logic block"(44) acts as a differential amplifier by subtracting the reset signals from the data output from the comparison/storage unit, column 3, line 64 through column 4, line 1. Data is output from logic block(44) to image storage and processing electronics(i.e. the outside), column 7, lines 17-21.).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

14. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gowda et al.(US 6,115,066) in view of Kim(US 6,423,957).

Consider claim 16, and as applied to claim 1 above, Gowda et al. teach a comparison/storage unit(see claim 1 rationale). However, Gowda et al. do not explicitly teach the internal contents of said comparison/storage unit.

Kim is similar to Gowda et al. in that Kim teaches a solid state imaging device(figure 4), comprising a pixel unit("pixel array", 20) formed on a semiconductor substrate and outputting, as an analog signal, a voltage signal corresponding to light(Column 2, lines 52-57) and a comparison/storage unit(30, figure 4), wherein transistors included in said pixel unit are all N-type MOS transistors(An AD converter(30) comprises a comparator(32), a double buffer(40), and a ramp voltage generator(31), figure 4. The AD converter(30) of figure 4 contains the same parts as the AD converter(30) of figure 1. These parts are detailed in figure 2, where a pixel(200) from the pixel unit is shown, and the comparator(320) and double buffer(400)

of the AD converter(30) are also shown. All of these devices similarly contain NMOS transistors alone, see figure 2.).

However, in addition to the teachings of Gowda et al., Kim teaches that the comparison/storage unit(30, figure 4, see figure 2) includes an inverter circuit having a booster circuit(See figure 2, the bottom portion clearly contains inverters and a booster circuit("PRECHARGE").).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to includes an inverter circuit having a booster circuit as taught by Kim in the comparison/storage unit taught by Gowda et al. for the benefit of aiding in the effective removal of unexpected pixel voltage in order to obtain a more desirable signal indicative of the actual object image(Kim, column 1, lines 52-55).

Allowable Subject Matter

15. Claim 10, 12, 13 and 15 are allowed.

16. The following is a statement of reasons for the indication of allowable subject matter:

Consider claim 10, the closest prior art, Kim et al.(6,423,957) teaches of a comparator(32, figure 4, 320, figure 2), and of a booster circuit(see claim 7 rationale). However, Kim et al. do not teach of fairly suggest that the comparator has an inverter circuit containing a booster circuit.

Consider claim 12, the closest prior art, Kim et al.(6,423,957) teaches of a memory(40, 400) and a booster circuit(see claim 7 rationale). Kim et al. further teach

that said memory(400) includes a plurality of switches(M5-M8, figure 2). However, Kim et al. do not teach of fairly suggest that said memory includes a capacitor or an output amplifier connected to a booster circuit.

Claim 13 is allowable as being dependant upon an allowable claim 12.

Consider claim 15, the closest prior art, Kim et al.(6,423,957) teaches of a counter generator("COUNT SIGNAL", figure 4), a pulse generator(31 figure 4), and a booster circuit(see claim 7 rationale). However, Kim et al. do not teach of fairly suggest that the said counter generator includes a plurality of inverter circuits each having a booster circuit.

17. Claims 2-6, 8, 11 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

18. The following is a statement of reasons for the indication of allowable subject matter:

Consider claim 2, the closet prior art, Gowda et al. (US 6,115,066) teaches a comparison/storage unit(see claim 1 rationale). However, Gowda et al. do not teach or fairly suggest that the comparison circuit is comprised of three inverter circuits including three N-type MOS transistors alone or serially connected, or that the resistance of various transistors is increased or decreased to increase the rise speed or fall speed of the inverters.

Claims 3-6, 8, 11 and 14 are allowable as being dependant upon an allowable claim 2.

Conclusion

19. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert H. Cutler whose telephone number is (571)-270-1460. The examiner can normally be reached on Mon-Fri (7:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ngoc-Yen Vu can be reached on (571)-272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AC

NGOC-YEN VU
SUPERVISORY PATENT EXAMINER